Description

A loop filter for a continuous time sigma delta analog to
digital converter

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The invention refers to a loop filter for a continuous time
sigma delta analog to digital converter.

The sigma delta analog to digital converters are among the
10    key components in modern electronics.

Continuous time (CT) sigma delta modulators can operate at a
higher sampling frequency than their discrete time (DT)
counterparts.

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Fig. 1 shows a continuous time sigma delta analog to digital
converter according to the state of the art. Continuous time
sigma delta analog to digital converters (CT $\Sigma\Delta$ ADC) are
widely employed in wireless communication receivers as well
20    as in sensor interfaces. The continuous time sigma delta
analog to digital converter according to the state of the art
as shown in Fig. 1 comprises two major components, i.e. a
loop filter and a quantizer.

25    Fig. 2 shows the loop filter of the conventional analog
digital converter in more detail. As can be seen from Fig. 2,
the loop filter according to the state of the art includes a
number of integrator elements which are connected in series
to each other. The output signal of each integrator element
30    is fed to the input of the next integrator element. Further,
the output signal of each integrator element may be coupled
via a feed-forward branch ($C_i$) to a summing point at the
output of the loop filter. In some loop filters, also feed-
back branches are provided. As shown in Fig. 2 the loop
35    filter of the conventional continuous time sigma delta analog
to digital converter comprises an input terminal and receives
the fed-back digital output signal of the analog-digital

converter ADC comprising m bits. The digital output signal is
supplied to at least one digital-analog converter (DAC1)
which converts the feed-back digital output signal to an
analog signal which is subtracted from the analog input
5    signal of the analog-digital converter (ADC). Further,
digital-analog converters (DAC2 ... DACn) can also be
implemented into the loop filter as shown in Fig. 2. In the
example given in Fig. 2, the conventional loop filter
comprises n-1 integrator stages and n digital-analog
10   converters. The order of the loop filter is n-1. In
conventional continuous time sigma delta analog to digital
converters filters having a filter order ranging from 2 to 7
are normally employed. The loop filters used in the
continuous time sigma delta analog to digital converter as
15   shown in Fig. 1 has an open loop gain which is necessarily
higher than one.

The transfer function of the loop filter as shown in Fig. 2
is defined by the ratio of the analog output signal of the
20   loop filter ($U_f$) and the digital input signal ($U_{outdig}$). For
each pole of the loop filter transfer function, an integrator
element is employed requiring an active device.

Whereas passive filters are built from passive components
25   such as resistors, capacitors and inductors, active filters
do not include inductors. Active filters also use resistors
and capacitors, but the inductors are replaced by active
devices capable of producing a power gain. These active
devices can range from simple transistors to integrated
30   circuits (IC), controlled sources such as operation
amplifiers (op amps) and operational transconductance
amplifiers (OTA), generalized impedance converters (GIC) and
frequency-dependent negative resistors (FDNR).

35   The voltage transfer function (VTF) is specified in the
frequency domain. The poles of the VTF correspond to the
roofs of its denominator polynomial. For each pole of the

voltage transfer function VTF, the loop filter according to the state of the art as shown in Fig. 2 employs an active device such as an operation amplifier or an operational transconductance amplifier (OTA). For each zero of the

5   voltage transfer function (VTF) of the loop filter, either a feed-forward branch (CI) or a feed-back digital-analog converter DAC is provided. In some loop filters, according to the state of the art, the feed-forward branches (CI) are built in those active elements such as voltage to current

10  converters.

The higher the filter order of the filter, the greater is the selectivity of said filter. To achieve a certain filter selectivity, it is necessary to employ a loop filter with a

15  certain filter order. When employing a loop filter according to the state of the art as shown in Fig. 2, the number of active devices provided within said loop filter is equal or even higher than the chosen filter order.

20  Since each active device consumes power, the power consumption of the analog-digital converter according to the state of the art as shown in Fig. 1 is increased with the filter order of the loop filter. Accordingly, a drawback of conventional continuous time sigma delta analog to digital

25  converters according to the state of the art as shown in Fig. 1 is that the power dissipation of such a conventional analog-digital converter is high.

Consequently, it is the object of the present invention to

30  provide a loop filter for a continuous time sigma delta analog to digital converter which minimizes the power dissipation of the analog-digital converter.

This object is achieved by a loop filter having the features

35  of main claim 1.

The invention provides a loop filter for a continuous time
sigma delta analog to digital converter which converts an
analog input signal to a digital output signal, said loop
filter comprising an active analog loop filter which includes
5      active devices for providing a power gain, wherein the number
of active devices of said active analog filter is lower than
the filter order of said active analog filter.

In a preferred embodiment, the active devices included in
10     said active analog filter are operational amplifiers.

In an alternative embodiment, the active devices of said
active analog filter are transconductance amplifiers.

15     In a further alternative embodiment, the active devices of
said active analog filter are voltage to current converters.

In a preferred embodiment, the active analog filter is a
cascaded analog filter, comprising cascaded analog filter
20     elements which are connected in series to each other.

In a preferred embodiment, the cascaded analog filter
elements are cascaded biquad filter elements.

25     In an alternative embodiment, the cascaded analog filter
elements are cascaded lattice filter elements.

In a preferred embodiment, at least one biquad filter element
is a Sallen and Key filter element.
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In a preferred embodiment, the loop filter comprises a first
input terminal for applying the analog input signal of said
analog-digital converter.

35     The loop filter comprises in a preferred embodiment an output
terminal for supplying the output signal of the loop filter
to a quantizer which quantizes the loop filter output signal

to generate said digital output signal of said analog digital converter.

In a preferred embodiment, the digital output signal is fed
5   back to a second input terminal of said loop filter.

In a preferred embodiment, the loop filter comprises at least one digital-analog converter (DAC) which converts the digital output signal applied to said second input terminal of said
10  loop filter into an analog signal.

In a preferred embodiment, the analog signal generated by said digital analog converter (DAC) is added to the analog input signal applied to said first input terminal of said
15  loop filter.

The invention further provides a continuous time sigma delta analog to digital converter which converts an analog input signal to a digital output signal, wherein the continuous
20  time sigma delta analog to digital converter comprises a loop filter which has an active analog filter which includes active devices providing a power gain,
wherein the number of active devices is lower than the filter order of the active analog filter, and
25  wherein the continuous time sigma delta analog to digital converter further comprises a quantizer which quantizes a loop filter output signal of said active loop filter to generate said digital output signal.

30  In a preferred embodiment of the continuous time sigma delta analog to digital converter, the loop filter comprises a first input terminal for applying the analog input signal.

In a preferred embodiment of the continuous time sigma delta
35  analog to digital converter, the digital output signal of the quantizer is fed back to a second input terminal of said loop filter.

In a further embodiment of the continuous time sigma delta
analog to digital converter, the loop filter comprises at
least one digital-analog converter which converts the digital

5    output signal applied to said second input terminal of the
loop filter into an analog signal.

In a still further embodiment of the continuous time sigma
delta analog to digital converter, the analog signal

10   generated by the digital-analog converter (DAC) is subtracted
from the analog input signal applied to the first input
terminal of said loop filter.

In the following preferred embodiments of the loop filter for

15   a continuous time sigma delta analog converter are described
in detail.

Fig. 1 shows a continuous time sigma delta analog converter
according to the state of the art;

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Fig. 2 shows a loop filter for a continuous time sigma delta
analog converter according to the state of the art;

Fig. 3 shows a preferred embodiment of the continuous time

25   sigma delta analog converter according to the present
invention;

Fig. 4 shows a conventional biquad filter element;

30   Fig. 5 shows a conventional Sallen and Key filter element of
filter order two;

Fig. 6 shows the VTF poles of the Sallen and Key second-order
filter elements as shown in Fig. 5;

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Fig. 7 shows a conventional Sallen and Key filter element of
filter order five;

Fig. 8 shows a cascaded analog filter comprising cascaded analog biquad filter elements as employed in the present invention;

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Fig. 9 shows a cascaded analog filter comprising cascaded analog biquad filter elements as employed in a preferred embodiment of the present invention;

10    Fig. 10 shows a third-order analog filter as employed in a preferred embodiment of the present invention;

Fig. 11 shows a fourth-order active filter as employed in a preferred embodiment according to the present invention;

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Fig. 12 shows a two input biquad filter which is employed in a preferred embodiment according to the present invention;

Fig. 13 shows the implementation of a continuous time sigma
20    delta analog converter according to a preferred embodiment of the present invention;

Fig. 14 shows the gain and phase response of the loop filter according to a preferred embodiment of the present invention
25    as shown in Fig. 13.

Fig. 3 shows a preferred embodiment of a continuous time sigma delta analog-digital converter 1 according to the present invention. The continuous time sigma delta analog-
30    digital converter 1 converts an analog input signal ($U_{in}$) which is applied to an input terminal 2 of said continuous time sigma delta analog-digital converter 1. The analog-digital converter 1 converts the analog input signal ($U_n$) to a digital output signal ($U_{outdig}$) which is output via an output
35    terminal 3 of the ADC_1. The continuous time sigma delta analog-digital converter 1 comprises two major components,

i.e. the loop filter 4 and a quantizer 5 for quantizing the
output signal of said loop filter 4.

The loop filter 4 has a first input terminal 6 which is

5     connected to the input terminal 2 of the continuous time
sigma delta analog-digital converter 1 via an internal line
7. The loop filter 4 further comprises a second input
terminal 8 which is connected via a line 9 to a line 10 which
connects an output 11 of the quantizer 5 to the output

10    terminal 3 of the continuous time sigma delta analog-digital
converter 1. By means of the feed-back lines 9, the digital
output signal generated by the quantizer 5 is fed back to the
second input terminal 8 of the loop filter 4.

15    The loop filter 4 comprises an active analog filter 12 having
an input 13 and an output 14. The output 14 of the active
analog filter 12 within the loop filter 4 is connected via an
internal line 15 to an output terminal 16 of said loop filter
4. The output terminal 16 of the loop filter 4 is connected

20    via a line 17 to an input 18 of the quantizer 5.

The loop filter 4 comprises at least one digital-analog
converter 19 having an input 20 connected to the second input
terminal 8 of the loop filter via a line 21. The digital-

25    analog converter 9 further comprises an analog output 22
which is connected via a line 23 to an adder 24 of the loop
filter 4. The adder 24 is further connected to the first
input terminal 6 of the loop filter 4 via line 25. The
digital-analog converter 19 converts the feed-back digital

30    output signal $U_{outdig}$ to an analog signal which is added by
means of said adder 24 to the analog input signal $U_{in}$ applied
to the input terminal 2 of the continuous time sigma delta
analog-digital converter 1. The continued feed-back loop
controls the digital output signal $U_{outdig}$ such that the

35    difference between the analog input signal $U_{in}$ and the
converted analog output signal output by said digital-analog
converter 19 is minimized. To achieve this, the active analog

filter 12 provides for a signal amplification, wherein the
open loop gain is higher than one. The gain of the active
analog filter 12 is frequency-dependent to achieve stability
of the regulating loop signal wherein a higher frequency

5    signal is more attenuated than signals with lower
frequencies. Accordingly, the active analog filter 12 forms
an analog low-pass filter or an analog bandpass filter.

The active analog filter 12 includes active devices for

10   providing the necessary power gain. These active devices are,
in a preferred embodiment, operational amplifiers. In an
alternative embodiment, the active devices within the active
analog filter 12 are formed by a transconductance amplifier
(OTA). In other embodiments, the active devices are formed by

15   voltage to current converters or any other active device
capable of producing power gain such as signal transistors or
impedance converters.

The active analog filter 12 comprises a predetermined filter

20   order N which is predetermined according to the application
of the continuous time sigma delta analog-digital converter
1. If the selectivity of the active analog filter 12 is
increased with increasing filter order N, according to the
present invention, the number M of active devices provided

25   within the active analog filter 12 is lower than the filter
order (N) of said active analog filter 12. By minimizing the
number of active devices within the active analog filter 12,
the power consumption of the loop filter 4 within the
continuous time sigma delta analog-digital converter 1 is

30   also minimized so that the power dissipation of the analog-
digital converter 1 according to the present invention is
very low.

      Fig. 4 shows a conventional biquad filter element according
35   to the state of the art.

The voltage transfer function VTF is given by:

$$VTF = \frac{G_1 \cdot G_3 + p(C_1 - c_1)G_3 + p^2 C_2 \cdot C_3}{G_2 \cdot G_3 + p \cdot C_2 \cdot G_4 + p^2 \cdot C_2 \cdot C_4} = \frac{U_{out}}{U_{in}} \qquad (1)$$

The RC-active filter capable of realizing a biquad voltage
transfer function, i.e. a transfer function whose numerator
and denominator polynomials are second order is called a
biquad filter.

The transfer function of a biquad filter is given by:

$$VTF_{BQ} = k \frac{(p + z_1)(p + z_2)}{(p + p_1)(p + p_2)} \qquad (2)$$

wherein $z_i$ in the numerator represents zeros and $p_i$ in the
denominator represent poles of the transfer function.

A biquad filter has two complex conjugate poles and two
complex conjugate zeros. Fig. 4 shows a conventional biquad
filter element of filter order two comprising two active
devices, i.e. op amp 1 and op amp 2. In the biquad filter
element shown in Fig. 4, the number of active devices is
equal to the filter order of the filter element.

There exist biquad filter elements wherein the number of
active devices employed is lower than the order of the filter
element. Such a biquad filter element is the Sallen and Key
filter element shown in Fig. 5. The voltage transfer function
VTF of the Sallen and Key filter element as shown in Fig. 2
is given by:

$$VTF_{slk} = \frac{k \dfrac{1}{C_1 C_2 R_1 R_2}}{p^2 + p\left[\dfrac{1}{C_2 R_2} + \dfrac{1}{C_2 R_1} + \dfrac{1-k}{C_1 R_1}\right] + \dfrac{1}{C_1 C_2 R_1 R_2}} \qquad (3)$$

wherein

$$K = 1 + \frac{Rx}{Ry} \qquad\qquad\qquad (4)$$

The Sallen and Key filter element as shown in Fig. 5 is a second-order filter element. The voltage transfer function
5    VTF indicates that the Sallen and Key filter element is an all-pole low-pass filter element, since the numerator involves only a constant term.

Fig. 6 shows the poles of the second-order Sallen and Key
10   filter element shown in Fig. 5.

As can be seen from Fig. 5, the Sallen and Key filter element is a biquad filter element of filter order two, but the number of active devices, i.e. the number of the operation
15   amplifiers within the Sallen and Key filter element, is only one.

Fig. 7 shows a further Sallen and Key filter element employing only one operation amplifier to realize a higher
20   order Sallen and Key filter element.

By cascading biquad filter elements, it is possible to form a filter of any order as shown in Fig. 8. For example, by cascading k Sallen and Key filter elements as shown in
25   Fig. 8, it is possible to build a filter having the filter order 2k. This filter only includes k active devices so that the power consumption of such a filter is comparatively low.

Fig. 9 shows a fourth-order filter which is formed by two
30   cascaded biquad filter elements. Each biquad filter element includes only one operational amplifier op amp. The voltage transfer function VTF of the filter shown in Fig. 9 comprises four poles and four real zeros.

35   If the active analog filter 12 has an odd filter order, a cascade of biquad filter elements is connected in series to a

one-poled analog filter as can be seen in Fig. 10. The third-
order active analog filter 12 as shown in Fig. 10 comprises
only two active devices, i.e. two op amps.

5   Fig. 11 is a further embodiment of an active analog filter 12
    comprising two cascaded filter elements 12-1, 12-2, wherein
    the first filter element 12-1 is a two-pole resonator and
    wherein the second filter element 12-2 is a two-pole two-zero
    Sallen and Key filter element having two inputs. By employing
10  a multiple input second filter element 12-2, the fourth-order
    active analog filter is realized without any feed-forward
    voltaged current converters, thus saving a further active
    device.

15  Fig. 12 shows a two-input biquad filter element which can be
    combined with a feed-forward topology as shown in Fig. 11.
    For the sake of simplicity, only one half of the symmetric
    circuit arrangement is depicted in Fig. 12.

20  Fig. 13 shows a preferred embodiment of the loop filter 4
    according to the present invention. The loop filter 4
    includes an active analog filter 12 as shown in Fig. 10. The
    active analog filter 12 is a third-order active analog filter
    which consists of two cascaded filter elements, i.e. a one-
25  pole filter element 12-1 and a two-pole two-zero biquad
    filter element 12-2. The third-order active element 12
    comprises only two operational amplifiers, i.e. the number of
    active devices in filter 12 is lower than the filter order of
    the filter 12.
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    Fig. 14 shows the signal and phase response of the active
    analog filter 12 as shown in Fig. 10. Within a passband
    frequency band ranging from 0 to 10 MHz, the analog filter 12
    has the gain of more than 38 dB. At the unity gain frequency
35  (48 MHz), the phase margin is approximately 50°. The passband
    frequency range of 0 to 10 MHz corresponds to the passband
    frequency band of VDSL applications. In ADSL applications,

the passband frequency range of the active analog filter 12
is chosen to be 0 to 2 MHz. The active analog filter forms
part of the loop filter 3 as can be seen in Fig. 13. The
digital-analog filter 19-n is optional and can be used for

5    stability enhancement. Stability enhancement is only required
when the oversampling inside the sigma delta loop is very
low.

Reference List

| 1  | continuous time sigma delta analog-digital converter |
|----|------------------------------------------------------|
| 2  | input terminal                                       |
| 3  | output terminal                                      |
| 4  | loop filter                                           |
| 5  | quantizer                                             |
| 6  | input terminal                                       |
| 7  | line                                                 |
| 8  | input terminal                                       |
| 9  | feed-back line                                       |
| 10 | line                                                 |
| 11 | output                                               |
| 12 | active analog filter                                 |
| 13 | input                                                |
| 14 | output                                               |
| 15 | line                                                 |
| 16 | output terminal                                      |
| 17 | line                                                 |
| 18 | input                                                |
| 19 | digital-analog converter                             |
| 20 | input                                                |
| 21 | output                                               |
| 22 | output                                               |
| 23 | line                                                 |
| 24 | adder                                                |
| 25 | line                                                 |